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10/789,117	02/27/2004	Louis B. Hobson	200314976-1	7606

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EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,117	HOBSON, LOUIS B.	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been presented for examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 02/27/04 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Drawings

3. Figures 1-8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1- 24 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Specifically, claims 1-13, and 23-24 are written so broadly that they can be directed towards software without the need for hardware and thus software per se.

Specifically, for claims 14-21, the current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a useful, concrete and tangible result. No physical transformation is recited and additionally, the final result of the claim is writing the bit pattern to the ACPI throttling register which is not a tangible or useful result because the bit pattern only exists within the processor and does not allow the usefulness of the result to be realized.

Specifically, claims 22 and 24 are directed to a signal directly or indirectly by claiming a medium and the Specification recites evidence ([0020]) where the computer readable medium is define as a "*wave*" (such as a carrier wave) . In that event, the claims are directed to a form of energy which at present the office feels does not fall into a category of invention. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101.

<http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf>

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 1, the phrase "may be written" renders the claim indefinite because it is unclear whether the limitation is given patentable weight. Claims 2-13 by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-4, 6-21, and 23-24 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by **Bhatia et al. (U.S. Patent No. 6,535,798 B1).**

As per claim 1, Bhatia is directed to a system for simulating a processor performance state, comprising: a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register, and a set of bit patterns that may be written to the ACPI throttling register **(column 12, lines 38-57)**, and a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns to be written to the ACPI throttling register, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 2, Bhatia is directed to the system of claim 1, where the data structure is further configured to store an address of an ACPI status register from which a value related to a throttling status established by the ACPI throttling register can be read **(column 12, lines 40-43)**.

As per claim 3, Bhatia is directed to the system of claim 1, where the memory is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions **(column 7, lines 57-65)**.

As per claim 4, Bhatia is directed to the system of claim 1, where the data structure comprises an ACPI table stored in a memory that is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions **(column 7, lines 57-65)**.

As per claim 6, Bhatia is directed to the system of claim 1, where the set of bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state **(column 5, lines 22-25)**.

As per claim 7, Bhatia is directed to the system of claim 1, where the set of bit patterns facilitates simulating four processor performance states **(column 8, lines 55-61)**.

As per claim 8, Bhatia is directed to the system of claim 1, where the set of bit patterns facilitates simulating two or more processor performance states **(column 9, lines 46-48)**.

As per claim 9, Bhatia is directed to the system of claim 8, where the two or more processor performance states include eight processor performance states simulated by throttling the processor 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time **(column 8, lines 55-61)**.

As per claim 10, Bhatia is directed to the system of claim 1, where the ACPI throttling register is configured to cause the processor to be throttled by asserting a signal on a line connected to the processor **(column 4, lines 8-24)**.

As per claim 11, Bhatia is directed to the system of claim 10, where the line comprises the STOPCLK# line **(column 13, lines 63-67)**.

As per claim 12, Bhatia is directed to a computer configured with a system for simulating a processor performance state, the system comprising: a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register and a set of bit patterns that may be written to the ACPI throttling register **(column 12, lines 38-57)**, and a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns to be written to the ACPI throttling register, and to cause the processor to be throttled in

a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 13, Bhatia is directed to a printer configured with a system for simulating a processor performance state, the system comprising: a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register and a set of bit patterns that may be written to the ACPI throttling register **(column 12, lines 38-57)**, and a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns to be written to the ACPI throttling register, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 14, Bhatia is directed to a method for simulating a processor performance state, comprising: receiving a request to establish a processor performance state in a processor **(column 12, lines 38-57)**; accessing a data structure to acquire a bit pattern to write to an ACPI throttling register and an address for the ACPI throttling register **(column 12, lines 38-57)**; and simulating a processor performance state by causing the processor to be throttled in response to writing the bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

As per claim 15, Bhatia is directed to the method of claim 14, including establishing the data structure as an ACPI table in a Basic Input Output System (BIOS) operably connectable to the processor **(column 7, lines 57-65)**.

As per claim 16, Bhatia is directed to the method of claim 15, where establishing the data structure includes writing a set of bit patterns to the ACPI table and writing the address of the ACPI throttling register to the ACPI table **(column 12, lines 40-43)**.

As per claim 17, Bhatia is directed to the method of claim 14, where the processor performance state corresponds to one of a higher performance state and a lower performance state **(column 5, lines 22-25)**.

As per claim 18, Bhatia is directed to the method of claim 14, where the processor performance state corresponds to one of two or more user defined processor performance states **(column 9, lines 46-48)**.

As per claim 19, Bhatia is directed to the method of claim 14, where the processor performance state corresponds to one of eight processor performance states including a state where the processor is throttled one of 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time **(column 8, lines 55-61)**.

As per claim 20, Bhatia is directed to the method of claim 14, where writing the bit pattern to the ACPI throttling register causes a signal to be asserted on a STOPCLK# line into the processor **(column 4, lines 8-24 and column 13, lines 63-67)**.

As per claim 21, Bhatia is directed to the method of claim 14, including: acquiring an address of an ACPI status register configured to report a value related to a throttling status of the processor **(column 12, lines 40-43)**; reading the value from the ACPI status register **(column 12, lines 40-43)**; and selectively reporting a success or error condition based on the value **(column 13, lines 8-18)**.

As per claim 23, Bhatia is directed to a system, comprising: means for accessing ACPI data **(column 12, lines 38-57)**; means for receiving a request to drive a processor into a processor performance state **(column 12, lines 38-57)**; and means for controlling a clock signal to the processor by writing data retrieved from the ACPI data to an ACPI throttling register, where controlling the clock signal simulates the processor performance state **(column 9, lines 12-26)**.

As per claim 24, Bhatia is directed to a set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with simulating a

processor performance state in a processor by controlling an ACPI throttling register, comprising: a first interface for communicating a bit pattern data **(column 12, lines 38-57)**; a second interface for communicating an ACPI throttling register address data; and a third interface for communicating a state data, where the state data is related to a simulated processor performance state generated by applying the bit pattern data to a register identified by the register address data **(column 9, lines 12-26)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 5 and 22 are** rejected under 35 U.S.C. 103(a) as being unpatentable over **Bhatia (U.S. Patent No. 6,535,798 B1).**

As per claim 5, Bhatia is directed to the system of claim 1, but fails to specifically disclose where the data structure comprises an ACPI table stored in a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions. However, Bhatia does disclose a data structure

comprising an ACPI table that is operable connected to a BIOS which is functionally equivalent to the above limitation **(column 7, lines 57-65)**.

As per claim 22, Bhatia is directed to a computer-readable medium storing processor executable instructions operable to perform a method for simulating a processor performance state in a processor, the method comprising: establishing an ACPI table in a Basic Input Output System (BIOS) operably connectable to the processor, where establishing the ACPI table includes writing a set of bit patterns to the ACPI table, and writing an address of an ACPI throttling register to the ACPI table **(column 12, lines 38-57)**; receiving a request to establish a processor performance state in the processor, where the processor performance state corresponds to one of a higher frequency state and a lower frequency state **(column 12, lines 38-57)**; accessing the ACPI table to acquire a bit pattern to write to the ACPI throttling register and an address for the ACPI throttling register **(column 9, lines 12-26)**; and causing a processor to simulate a processor performance state by throttling the processor by writing the bit pattern to the ACPI throttling register **(column 9, lines 12-26)**.

Although Bhatia does not specifically disclose establishing an ACPI table in BIOS, it does disclose a data structure comprising an ACPI table that is operable connected to a BIOS which is functionally equivalent to the above limitation **(column 7, lines 57-65)**.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

1. U.S. Patent No. 7,082,542 B2 issued to Cooper on 07/25/06.
2. U.S. Patent No. 6,122,748 issued to Hobson on 09/19/00.

9. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suzanne Lo
Patent Examiner
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SL
07/31/06

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SUPERVISORY PATENT EXAMINER